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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/613,006	07/07/2003	Scot A. Kellar	42P12750D	4498

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EXAMINER	
DOLAN, JENNIFER M	

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/613,006	KELLAR ET AL.	
	Examiner	Art Unit	
	Jennifer M. Dolan	2813	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 May 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *25* is/are allowed.

6)☒ Claim(s) *1-3,7,9,10,14,16-18,21,23 and 24* is/are rejected.

7)☒ Claim(s) *4-6,8,11-13,15,19,20 and 22* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 5/26/05 has been entered.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claim 23 is rejected under 35 U.S.C. 102(e) as being anticipated by U.S. Patent Publication No. 2002/0163072 to Gupta et al. (cited by applicant).

Gupta teaches selectively depositing a plurality of metallic lines (210, 211) on opposing surfaces of adjacent wafers (see figures 8-11), wherein the adjacent wafers include a first and second wafer (paragraphs 0030-0031) and the plurality of metallic lines (paragraphs 0023, 0030) are surrounded by a dielectric recess to ensure that the metallic lines on the first wafer contact

the lines on the second wafer (paragraph 0029; figures 6-11); selectively aligning the wafers to form a stack (paragraph 0030); and bonding the metallic lines to electrically connect the active IC devices on the adjacent wafers (paragraphs 0021, 0030-0031).

4. Claim 24 is rejected under 35 U.S.C. 102(b) as being anticipated by U.S. Patent No. 5,401,672 to Kurtz et al.

Kurtz discloses depositing first and second barrier lines (portion '39' of layer 38; see figures 1 and 2c) on an outer edge (since the outer periphery of barrier 39 surrounds all active dice, it is considered to be at an "outer edge" of the wafer; see figure 2c) of a surface of first and second wafers (wafer 12a-12d, for example), the wafers having a plurality of dice (each region 40 in figure 2c; column 4, lines 35-50); and bonding the first and second barrier lines to bond the first and second wafers and form a barrier structure at the outer edge of the bonded wafer (column 2, lines 37-63; column 5, lines 10-20; figure 1).

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 2, 7, 9, 10, 14, 16-18, and 21, rejected under 35 U.S.C. 103(a) as being unpatentable over U.S. Patent No. 6,355,501 to Fung et al. (cited by applicant) in view of U.S. Patent No. 5,699,611 to Kurogi et al.

Fung discloses a wafer bonding method to form integrated chips corresponding to a single die (figures 5, 6, 9), comprising: selectively depositing a plurality of metallic lines (Cu; column 3, lines 10-15; figures 5-9; column 6, lines 15-30) on opposing surfaces of adjacent wafers (figure 9); selectively aligning the wafers to form a stack (figures 7-9); and bonding exposed portions of the metallic lines on the opposing surfaces of the adjacent wafers (column 6, lines 30-50) to establish electrical connections between active IC devices on the adjacent wafers (column 2, lines 15-20; figure 9). Fung further discloses depositing a barrier line on outer edges of the adjacent wafers, such that a barrier structure is present at the periphery of the wafer stack structure (column 5, line 55 – column 6, line 12) and such that the barrier protects the die from environmental contamination (column 5, lines 55-60).

Fung fails to teach that the barrier structure is formed by depositing barrier lines on the outer edge of each of the opposing surfaces of the wafers and then bonding the barrier lines together.

Kurogi teaches a wafer bonding method wherein a barrier against environmental contamination (column 1, lines 22-55) is formed by depositing copper (column 2, lines 38-39; column 3, lines 33-34) barrier lines (24, 40) on an outer edge of each opposing surface of adjacent wafers (figure 4) and then bonding the adjacent barrier lines as well as copper metallic lines (see column 2, lines 59-60) to each other (column 1, line 40-50; column 3, lines 1-36).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the barrier structure of Fung, such that it is formed in the manner suggested by Kurogi. The rationale is as follows: A person having ordinary skill in the art would have been motivated to use the methodology of Kurogi in forming the edge sealing barrier structure in the device of Fung, because the barrier structures in Fung and Kurogi perform substantially similar functions of sealing the edge of bonded wafers in order to protect the stacked wafer structure from contamination or other environmental hazards. The mutual bonding of barrier lines deposited on opposing faces of the chips, as in Kurogi, would be seen as advantageous to a person having ordinary skill in the art, because Kurogi specifically teaches that such a method is advantageous over the encapsulation type sealing method of Fung (see Kurogi, column 1, lines 30-40), in that it causes the barrier seal to automatically be formed when bonding the wafers and the electrical contact portions, and thus eliminates the need for a separate edge-sealing step (see Kurogi, column 1, lines 53-63).

7. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Fung et al. in view of Kurogi et al. as applied to claim 1 above, and further in view Gupta et al.

Fung fails to disclose that the metallic lines are surrounded by a dielectric recess.

Gupta discloses a stacked wafer IC similar to that of Fung (see figure 9 of Gupta), wherein the metallic lines bonded between two adjacent wafers are surrounded by a dielectric recess (paragraphs 0029-0030; figures 6-11).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the method of Fung as modified by Kurogi, such that the metallic lines are

surrounded by a dielectric recess, as suggested by Gupta. The rationale is as follows: A person having ordinary skill in the art would have been motivated to provide a dielectric recess surrounding the metal contacts, because doing so elevates the metal contact relative to the surrounding dielectric, such that improved bonding between adjacent wafers is achieved (see Gupta, paragraphs 0029-0030).

Allowable Subject Matter

8. Claim 25 is allowed.

9. Claims 4-6, 8, 11-13, 15, 19, 20, and 22 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

These claims are allowable for reasons deemed to be of record (Office Action of 4/12/05; Applicant's remarks of 5/26/05).

Response to Arguments

10. Applicant's arguments with respect to claims 1-25 have been considered but are largely moot in view of the new grounds of rejection.

Regarding claim 24, the Applicant has stated that the claim should be allowable based on the Examiner's reasons for allowability in the Office Action of 4/12/05. The Examiner would like to respectfully point out that the feature of having a barrier surrounding multiple dice has only been indicated as allowable in combination with the limitations of the independent claims and not as a separately claimed feature. Hence, claim 24 can be considered anticipated by

references such as Kurtz et al, as applied supra, while claim 4 is allowable, based on the inapplicability of Kurtz to structures having bonded metallic lines or based on the fact that the semiconductor-based barrier layers of Kurtz would not necessarily provide environmental or crack propagation protection during a cleaving process.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jennifer M. Dolan whose telephone number is (571) 272-1690. The examiner can normally be reached on Monday-Friday 8:30am-5:00pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl W. Whitehead, Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jennifer M. Dolan
Examiner
Art Unit 2813

jmd

Carl Whitehead

CARL WHITEHEAD, JR
SUPERVISORY PATENT EXAMINER
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